BLL2620

28V, 5A, 150KHz-ADJ Synchronous Step-Down DC/DC Converter

DESCRIPTION

The BLL2620 is a synchronous rectified step-down converter that provides wide 5V to 28V input voltage range and 5A continuous load current capability. The BLL2620 can operate at PFM mode to achieve high efficiency which can be programmed by a resistor tied between RT to ground and reduce power loss at light load. The COMP pin allows the loop compensation of the switching regulator to be optimized based on the programmed switching frequency, allowing for a fast transient response.

The BLL2620 protection function includes cycle-by-cycle current limit, hiccup short circuit protection, UVLO and thermal shutdown. Besides, internal soft-start prevents inrush current at fast power-on.

The BLL2620 requires a minimum number of readily available standard external components and is available in QFN4X4-14 package and provides good thermal conductance

FEATURES

- Low $R_{DS(ON)}$ integrated power MOSFET (25mΩ Typ)
- Wide input voltage range: 5V to 28V
- Adjustable output voltage down to 0.8V
- 5A output current
- Output Soft-Start and Power Good
- High efficiency at light load
- Cycle-by-cycle current limit
- Over-temperature protection with auto recovery
- Under voltage lockout
- Hiccup short circuit protection
- ADJ switch frequency from 150KHz
- Available in QFN4X4-14L package
- RoHS compliant

APPLICATIONS

- Distributed power system
- Flat panel television and monitors
- Wireless chargers
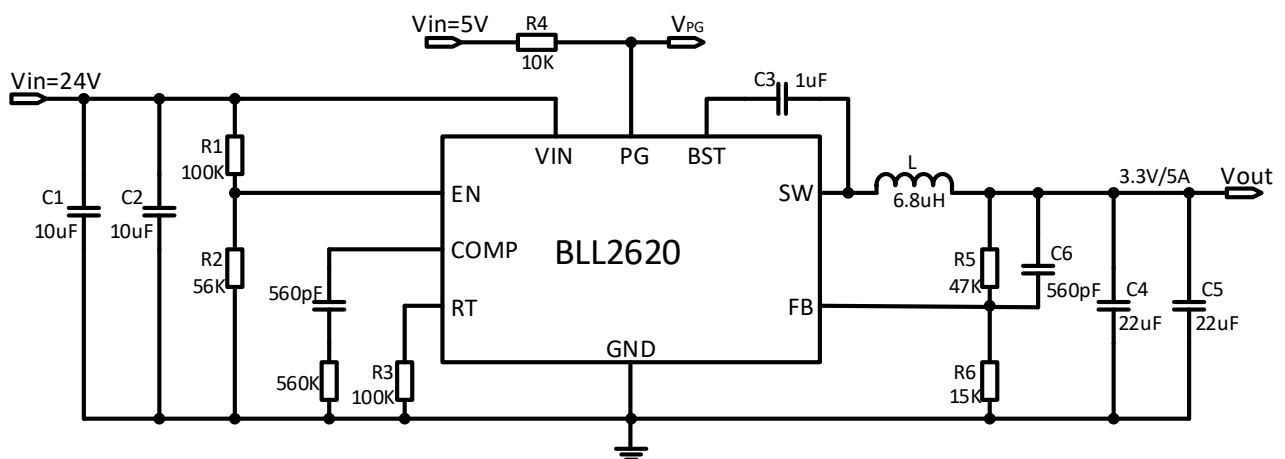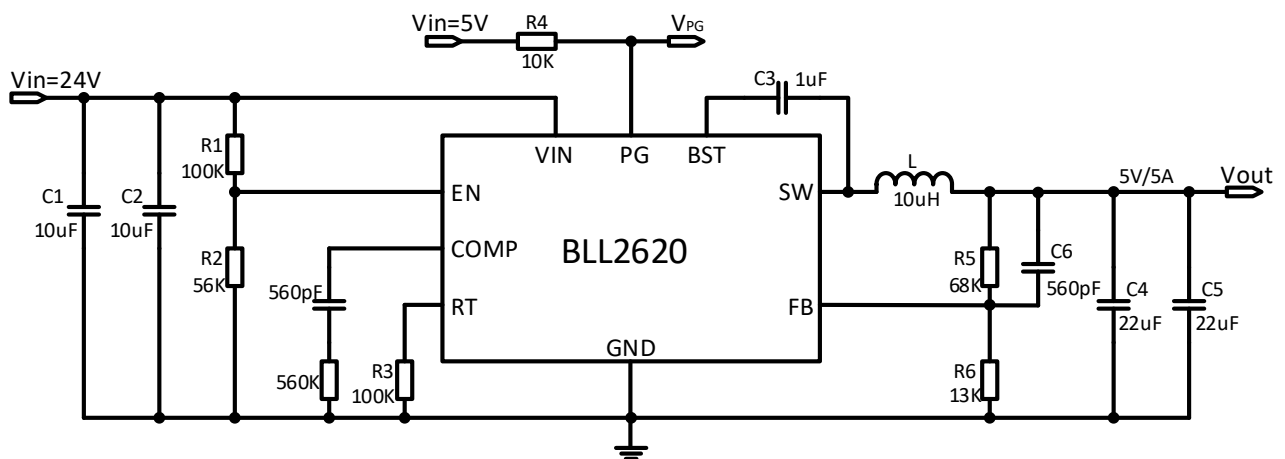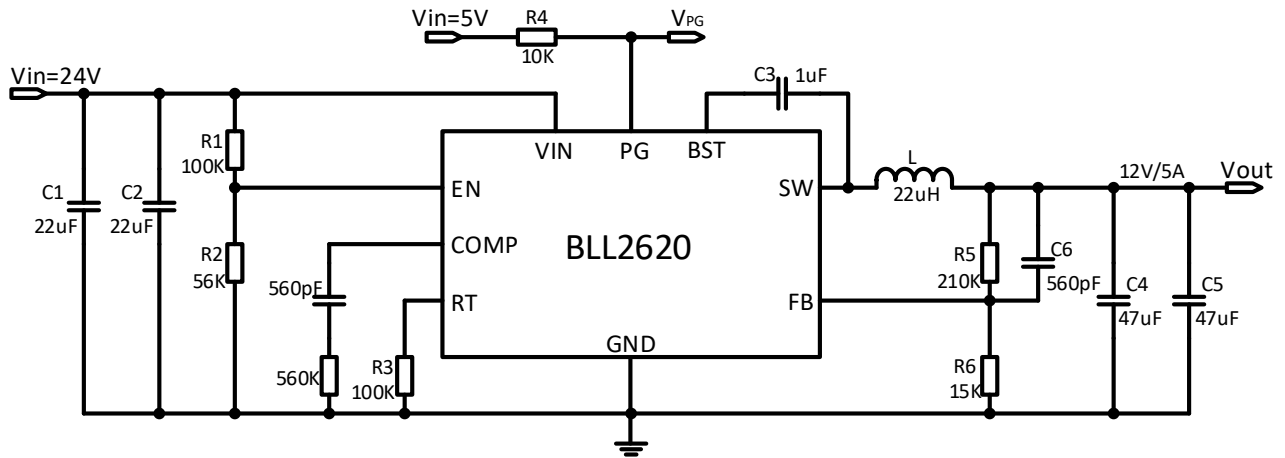- Networking, XDSL modem

PIN OUT & MARKING
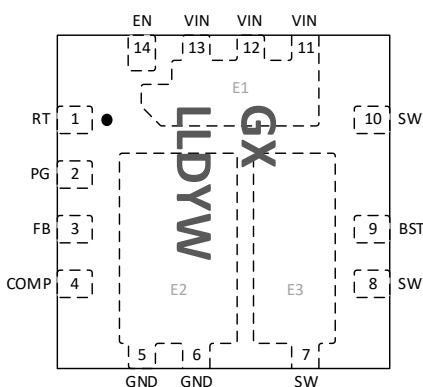
QFN 4X4-14

BLL2620CJHTR
GX: Product Code
LL: Lot No.
D: Fab code
YW: Date code

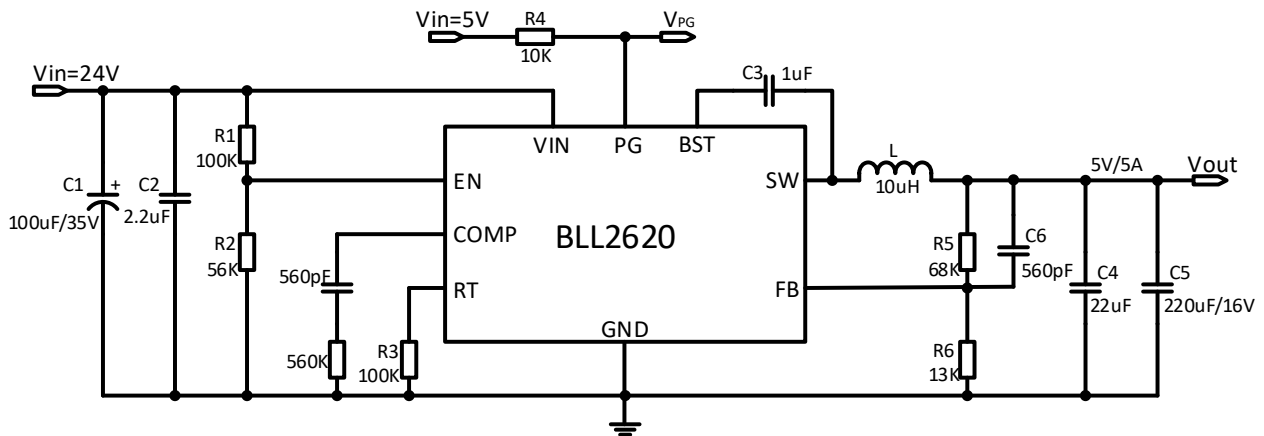## ORDERING INFORMATION

BLL2620 [1] [2] [3]	
[1]	Temperature&Rohs: C:-40~85°C ,Pb Free Rohs Std.
[2]	Package type: JH: QFN4X4-14
[3]	Packing type: TR:Tape&Reel (Standard)

BLL2620

TYPICAL APPLICATION

C_{IN} &C_{OUT} use Ceramic Capacitors Application Circuit

BLL2620

Vin=5V R4 10K V_PG

Vin=24V

C1 100uF/35V + C2 2.2uF

R1 100K

R2 56K

560pF

560K

R3 100K

VIN PG BST

EN

COMP **BLL2620**

RT

FB

GND

C3 1uF

SW L 10uH 5V/5A Vout

R5 68K C6 560pF C4 22uF C5 220uF/16V

R6 13K

C_{IN} &C_{OUT} use Electrolytic Capacitors Application Circuit

Note: *1) If the input voltage is below 12V, R1 can be set to 0K and R2 can be removed.*

2) R3 can be used to set the switch frequency of BLL2620. The detail information can be found at page 10.

Table1. Recommended Component Values

V_{IN}=12~24V, R3=100K, the recommended BOM list is shows as below.

V_{OUT}	C1	C2	C3	C6	L	R5	R6	C4	C5
12V	22uF/MLCC	22uF/MLCC			10uH-22uH	210K	15K	47uF/MLCC	47uF/MLCC
5V					4.7uH-10uH	68K	13K		
3.3V					3.3uH-6.8uH	47K	15K		
2.5V	10uF/MLCC	10uF/MLCC			3.3uH-6.8uH	39K	18K	22uF/MLCC	22uF/MLCC
1.8					2.2uH-4.7uH	15K	12K		
1.2					2.2uH-4.7uH	7.5K	15K		
12V			0.1~1uF	560pF~1nF	10uH-22uH	210K	15K		
5V					4.7uH-10uH	68K	13K		
3.3V					3.3uH-6.8uH	47K	15K		
2.5V	100uF/35V/ECL	2.2uF/MLCC			3.3uH-6.8uH	39K	18K	2.2uF/MLCC	220uF/16V/ECL
1.8					2.2uH-4.7uH	15K	12K		
1.2					2.2uH-4.7uH	7.5K	15K		

PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	RT	Pin used to program Switch Frequency by a resister to GND
2	PG	Open drain Power Good Indicator Output .Pulled up to 5V by a 10Kohm resistance.
3	FB	Feedback input with reference voltage set to 0.8V.
4	COMP	This pin is the error-amplifier output and the input to the PWM comparator. Connect frequency compensation components to this pin.
5, 6	GND	Ground.
7, 8, 10	SW	Power switching node to connect inductor.
9	BST	High side power transistor gate drive boost input.
11, 12, 13	VIN	Power input. Bypass with a 22uF ceramic capacitor to GND.
14	EN	Enable input. Set this pin to high level to enable the part, low level to disable.

BLL2620

ABSOLUTE MAXIMUM RATING

Parameter	Value
Supply voltage V_{IN}	-0.3V to 30V
Switch node voltage V_{SW}	-0.3V to (V_{IN}+0.5V)
Boost voltage V_{BST}	V_{SW}-0.3V to V_{SW}+5V
Enable voltage V_{EN}	-0.3V to 12V
The others pins	-0.3V to 6V
Operating temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C
Lead temperature (soldering, 10s)	260°C

Note: Exceed these limits to damage to the device. Exposure to absolute maximum rating conditions may affect device reliability.

RECOMMENDED WORK CONDITIONS

Item	Min	Recommended	Max.	Unit
Supply voltage V_{IN}	5		28	V
Ambient temperature	-40		85	°C

ELECTRICAL CHARACTERISTICS

(V_{IN}=12V, T_A=25°C, unless otherwise stated)

Parameter	Conditions	Min	Typ	Max	Unit
Input voltage range		5		28	V
UVLO threshold	V_{IN} rising		4.5		V
UVLO hypothesis	V_{IN} falling		250		mV
Supply current in operation	V_{EN} = 5V		250		uA
Supply current in shutdown	V_{EN} = 0V or V_{EN} = GND		3		uA
Regulated feedback voltage	4.2V≤V_{IN} ≤30V	0.784	0.800	0.816	V
High-side switch on resistance	V_{BST-SW} = 5V		25		mΩ
Low-side switch on resistance	V_{IN} = 5V		25		mΩ
High-side switch leakage current	V_{EN} = 0V, V_{SW} = 0V		0	10	uA
Upper switch current limit	50% duty cycle		7.5		A
Oscillation frequency	With R3 is NC		150		KHz
Minimum on time			100		ns
Minimum off time			200		ns
Soft start time			1.8		ms
Recommended duty cycle	R3=100KΩ	10		80	%
EN input voltage "H"		1.5			V
EN input voltage "L"				0.6	V
Thermal shutdown			160		°C
Thermal shutdown hysteresis			25		°C

ELECTRICAL PERFORMANCE

Efficiency vs. Iout
(Vout=1.2V)
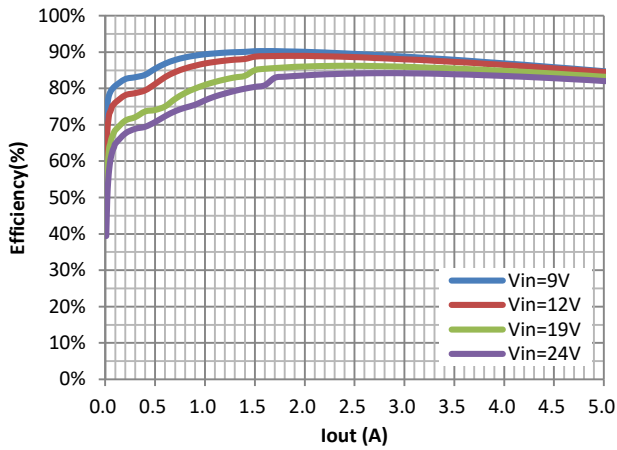
Vout vs. Iout
(Vout=1.2V)
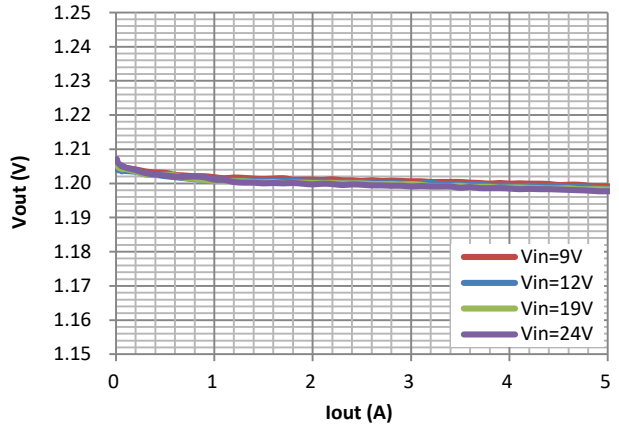
Efficiency vs. Iout
(Vout=3.3V)
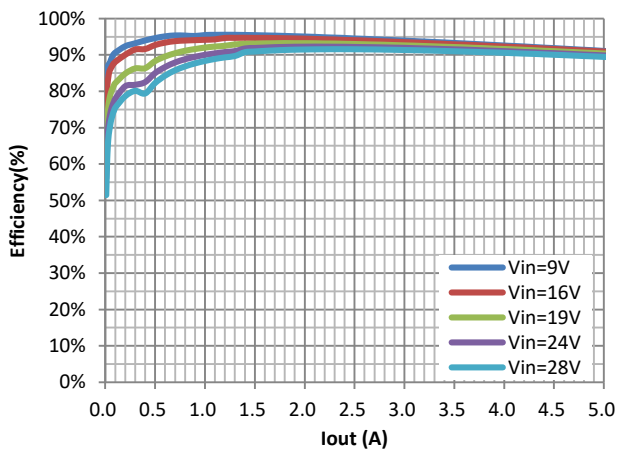
Vout vs. Iout
(Vout=3.3V)
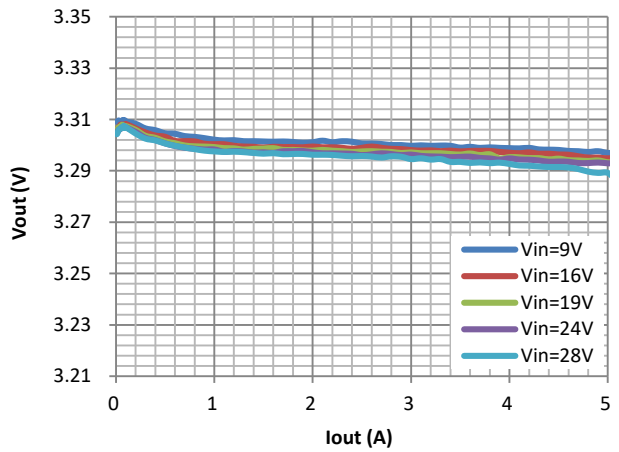
Efficiency vs. Iout
(Vout=5V)
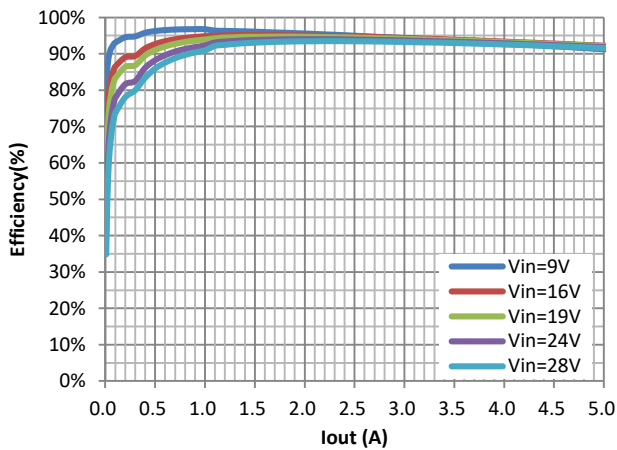
Vout vs. Iout
(Vout=5V)
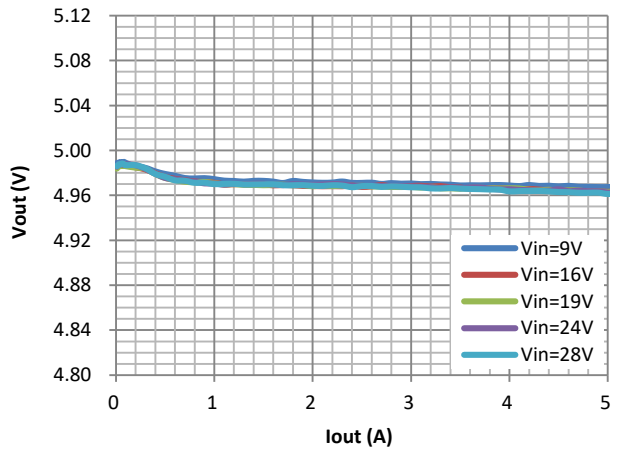
Efficiency vs. Iout
(Vout=12V)
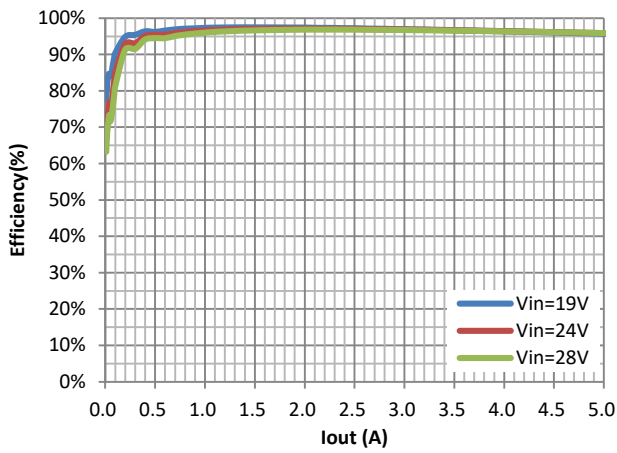
Vout vs. Iout
(Vout=12V)
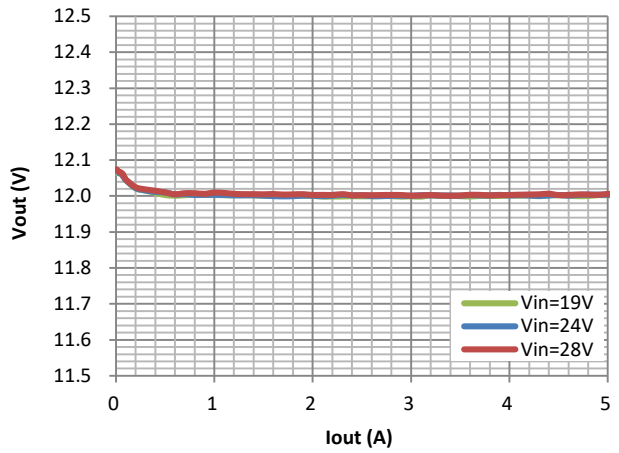
IQ
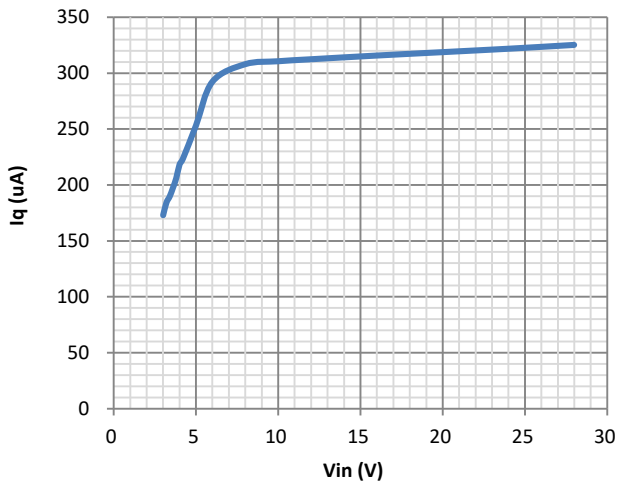
Switch Freq vs. RT

EN Power On
Vin=12V, Vout=5V, IL =3A, EN=0V to5V

Ch1—EN, Ch2—Vout, Ch3—SW, Ch4—IL

EN Power Off
Vin=12V, Vout=5V, IL =3A, EN=5V to 0V

Ch1—EN, Ch2—Vout, Ch3—SW, Ch4—IL

BLL2620
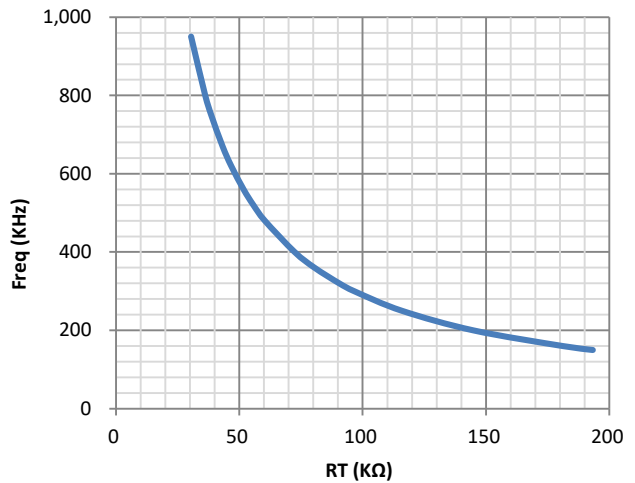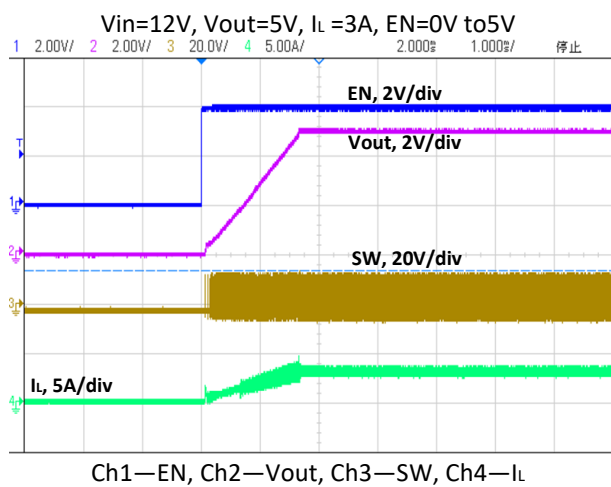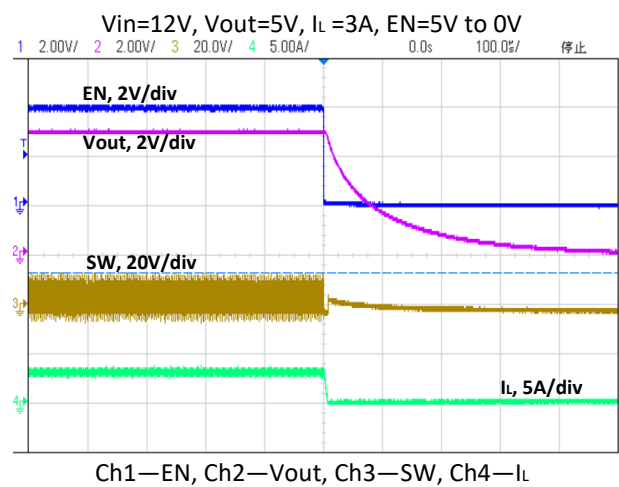
Load Transient
Vin=12V, Vout=5V, Iout=0.5A~4.5A, Cff=560pF

Vout ripple, 200mV/div

Iout, 5A/div
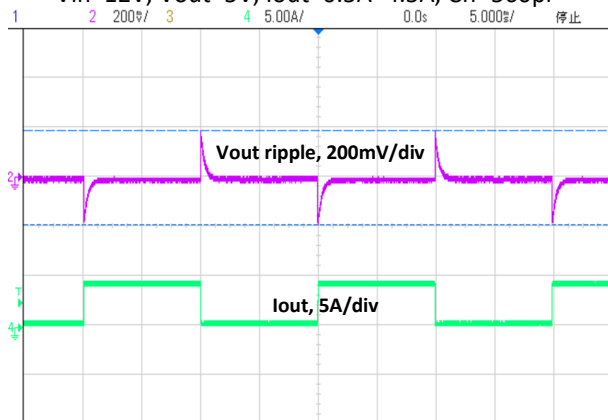
Ch2—Vout ripple, Ch4—Iout

Load Transient
Vin=24V, Vout=12V, Iout=0.5A~4.5A, Cff=560pF

Vout ripple, 200mV/div

Iout, 5A/div
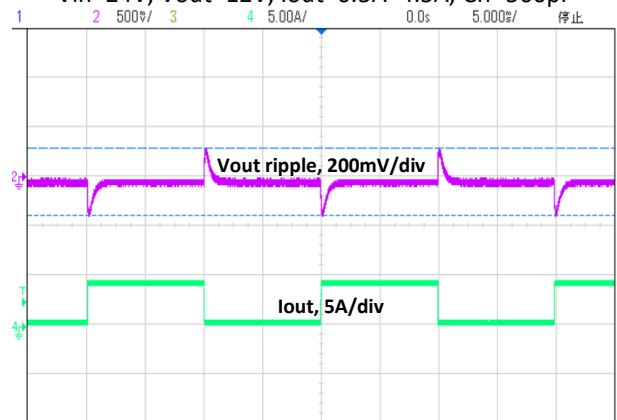
Ch2—Vout ripple, Ch4—Iout

Output Ripple Wave
Vin=12V, Vout=5V, I_L=0A
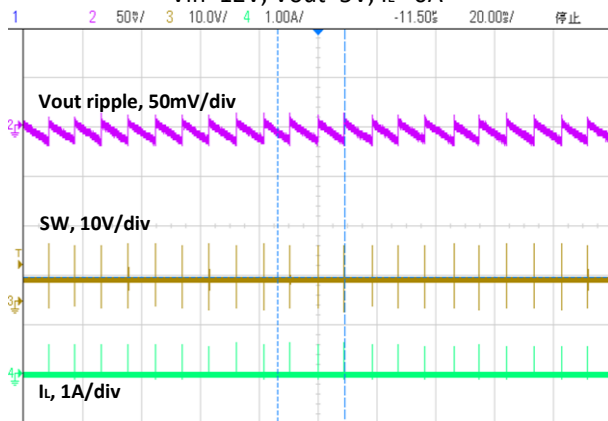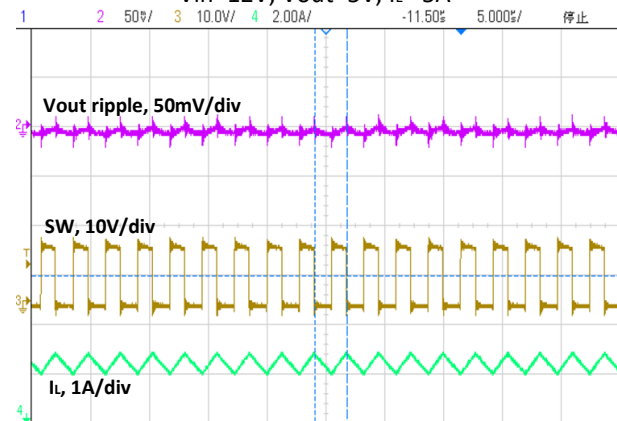
Vout ripple, 50mV/div

SW, 10V/div

I_L, 1A/div

Ch2—Vout, Ch3—SW, Ch4—I_L

Output Ripple Wave
Vin=12V, Vout=5V, I_L=5A

Vout ripple, 50mV/div

SW, 10V/div

I_L, 1A/div

Ch2—Vout, Ch3—SW, Ch4—I_L

Output Ripple Wave
Vin=24V, Vout=12V, I_L=0A

Vout ripple, 50mV/div

SW, 10V/div

I_L, 1A/div

Ch2—Vout, Ch3—SW, Ch4—I_L

Output Ripple Wave
Vin=24V, Vout=12V, I_L=5A

Vout ripple, 50mV/div

SW, 10V/div

I_L, 1A/div

Ch2—Vout, Ch3—SW, Ch4—I_L

Short Circuit Wave
Vin=24V, Vout=12V

Vout, 5V/div

SW, 10V/div

I$_L$, 5A/div

Ch2—Vout, Ch3—SW, Ch4—I$_L$

Short Circuit Wave
Vin=24V, Vout=12V

Vout, 5V/div

SW, 10V/div

I$_L$, 5A/div
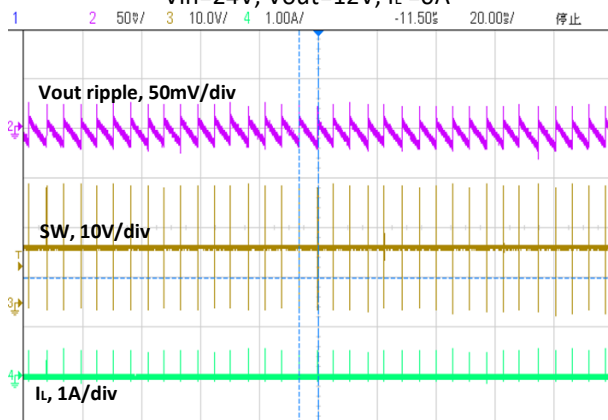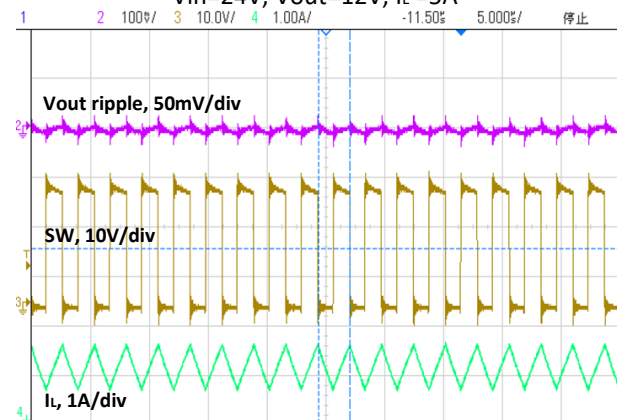
Ch2—Vout, Ch3—SW, Ch4—I$_L$
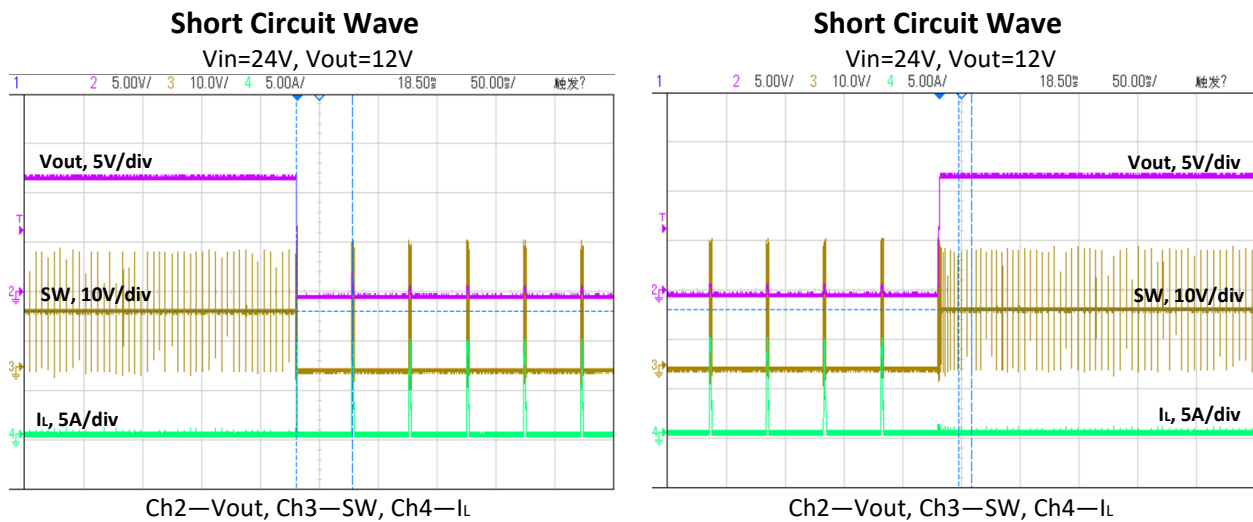
BLOCK DIAGRAM
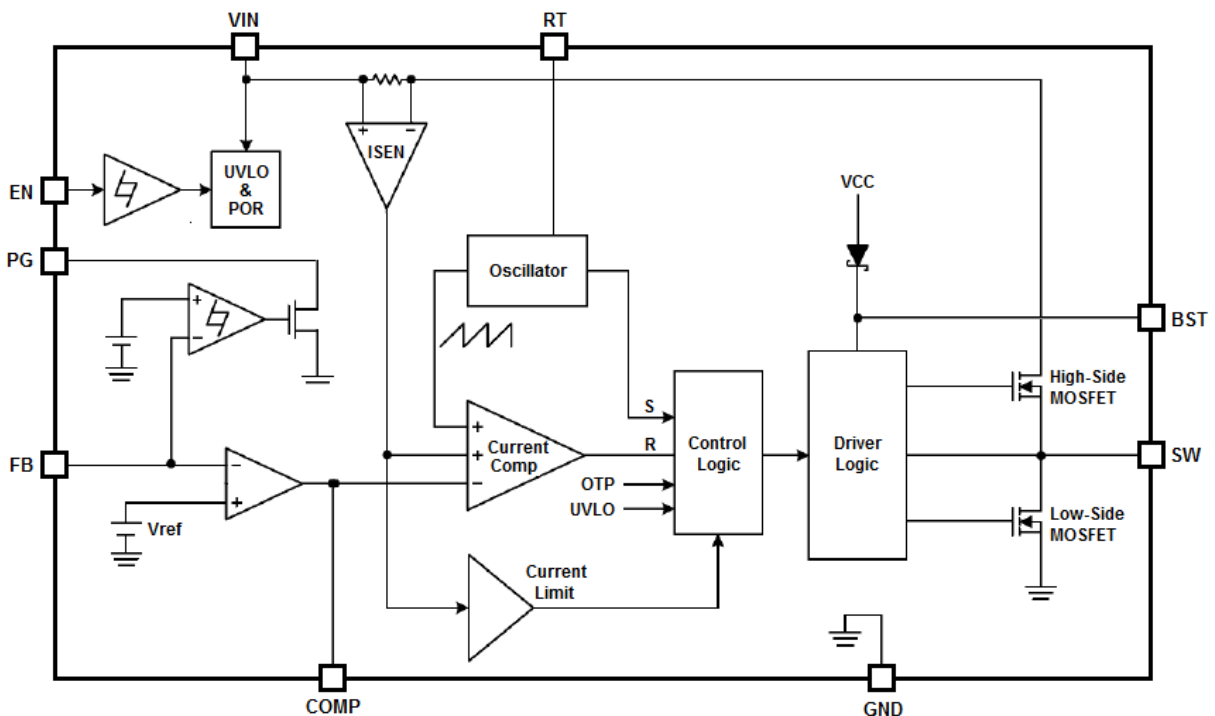
FUNCTIONAL DECRIPTIONS

Loop operation

The BLL2620 is a wide input range, high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 5A of output current, integrated with a 25mΩ synchronous MOSFET pair, eliminating the need for external diode. It uses a PWM current-mode control scheme. An error amplifier integrates error between the FB signal and the internal reference voltage. The output of the integrator is then compared to the sum of a current-sense signal and the slope compensation ramp. This operation generates a PWM signal that modulates the duty cycle of the power MOSFETs to achieve regulation for output voltage.

Internal soft-start

The soft-start is important for many applications because it eliminates power-up initialization problems. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

Over-current-protection and hiccup

The BLL2620 has a cycle-by-cycle over-current limit for when the inductor current peak value exceeds the set current-limit threshold. First, when the output voltage drops until FB falls below the Short-Voltage threshold (typically 300mV) to trigger a Short-Voltage event, the BLL2620 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current to alleviate thermal issues and to protect the regulator. The BLL2620 exits hiccup mode once the overcurrent condition is removed.

Light load operation

Traditionally, a fixed constant frequency PWM DC-DC regulator always switches even when the output load is small. When energy is shuffling back and forth through the power MOSFETs, power is lost due to the finite RDSONs of the MOSFETs and parasitic capacitances. At light load, this loss is prominent and efficiency is therefore very low. BLL2620 employs a proprietary control scheme that improves efficiency in this situation by enabling the device into a power save mode during light load, thereby extending the range of high efficiency operation.

Startup and shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATIONS INFORMATION

Setting output voltages

The external resistor divider is used to set the output voltage. The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. R2 is then given by:

$$R_2 = \frac{R_1}{V_{out}/V_{FB} - 1}$$
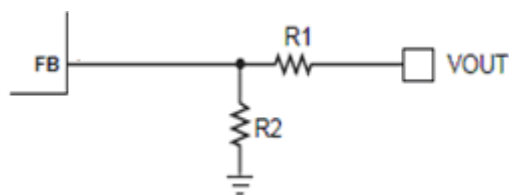
Selecting the inductor

Use a 2.2µH-to-10µH inductor with a DC current rating of at least 25% higher than the maximum load current for most applications. For most designs, derive the inductance value from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{osc}}$$

Where ΔIL is the inductor ripple current. Choose an inductor current approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light-load conditions (below 100mA), use a larger inductor to improve efficiency.

Selecting the output capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times R_{ESR}$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C_2} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The BLL2620 can be optimized for a wide range of capacitance and ESR values.

Setting the switch frequency

The switch frequency of BLL2620 can be programmed by a resistance R3 mentioned in the typical application at the page 2. The relationship

between the switch frequency and resistance of R3 is approximately given：

$$Freq(KHz) = \frac{29000}{R_3(K\Omega)}$$

A detailed design table about the relationship above is given for a conveniently reference：

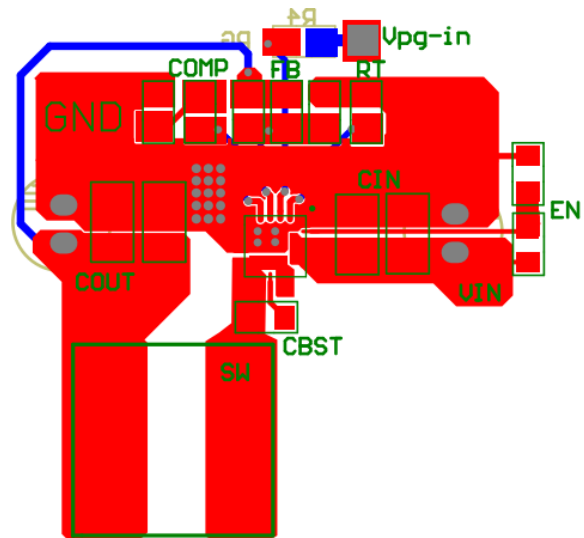| R(K)	F$_{SW}$(KHz)
30	950
39	750
51	560
62	480
75	400
91	320
100	300
NC	150

PCB LAYOUT RECOMMENDATION

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

1) Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2) Place feedback resistors close to the FB pin.
3) Keep the sensitive signal (FB) away from the switching signal (SW).
4) The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connecting to the

exposed pad should be maximized to improve thermal performance.
5) Multi-layer PCB design is recommended.

BLL2620

PACKAGE OUTLINE

Package	QFN4x4-14	Devices per reel	3000pcs

Package dimension:

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.55	0.65	0.75
e1	1.20	1.30	1.40
K	0.10	0.20	0.30
K1	0.15	0.25	0.35
K2	0.63	0.73	0.83
L	0.30	0.40	0.50
L1	2.225	2.325	2.425
L2	2.425	2.525	2.625
L3	0.775	0.875	0.975
L4	1.375	1.475	1.575
L5	0.975	1.075	1.175
L6	0.775	0.875	0.975
L7	1.87	1.97	2.07
L8	0.22	0.32	0.42
M	0.30	0.40	0.50
R	0.10	–	–

Unit: mm