上海贝岭 SHANGHAI BELLING

BLL2683

70V High Efficiency Synchronous Step-Down DC/DC Converter

DESCRIPTION

BLL2683 is a high efficiency, monolithic synchronous step-down DC/DC converter utilizing Jitter Function frequency, average current mode control architecture. Capable of delivering up to 3A continuous load with excellent line and load regulation. The device operates from an input voltage range of 7V to 70V and provides an adjustable output voltage from 3V to 40V.

In conclusion, BLL2683 is a full function and high performance, high reliability buck DC-DC converter.

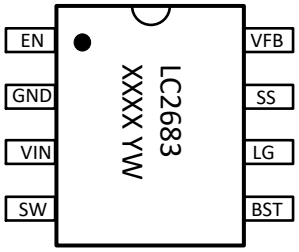
FEATURES

- Internal high-side and external low-side MOSFET
- Max output current: 3A
- Adjustable output voltage, V_{FB}=1V
- Constant voltage accurate: ±2%
- No external compensation needed
- Jitter function
- Efficiency: up to 94%
- Short circuit protection
- Thermal shutdown protection
- Under voltage lock-out
- Available in SOP-8 package

APPLICATIONS

- Distributed power systems
- Networking systems
- POE
- Industry application

PIN OUT & MARKING



SOP-8

LC2683: Product code
XXXX: Lot No.
YW: Date code (year & week)

ORDERING INFORMATION

Part No.	Package	Tape&Reel
BLL2683CD8TR	SOP8	4000pcs/reel

TYPICAL APPLICATION

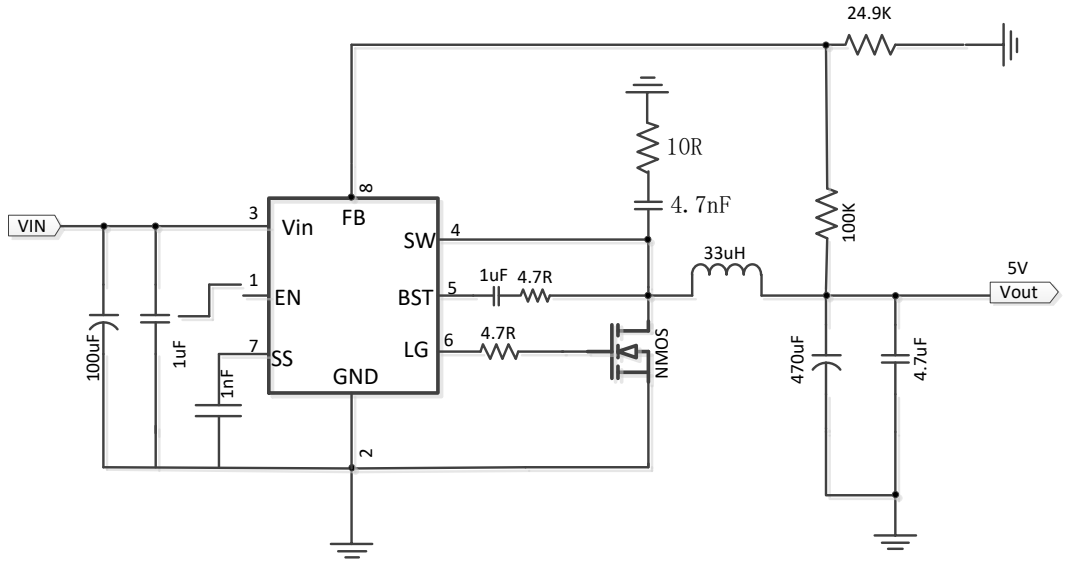


Figure 1

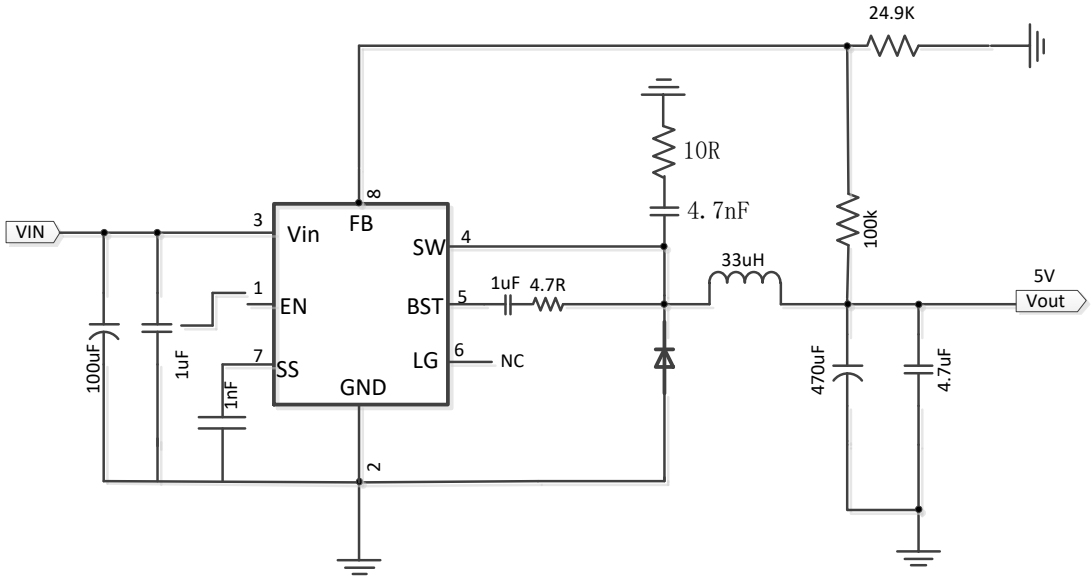


Figure 2

PIN DESCRIPTION

Pin #	Name	Description
1	EN	Enable input. Setting it to high level or Float may turn on the chip, while setting it to ground level will turn off the chip.
2	GND	Ground.
3	VIN	Power supply input. Place a 1μF ceramic capacitor between VIN and GND as close as possible.
4	SW	Power switching output connect to external inductor.
5	BST	Connect a 1uF capacitor between BST and SW pin to supply current for the top switch driver.
6	LG	Driver of Low side NMOS, Connect to the gate of NMOS.
7	SS	Soft-start node. Connecting a 1nF capacitor to ground make the Buck converter output rise smoothly.
8	FB	Feedback voltage.

ABSOLUTE MAXIMUM RATING

Parameter		Value
VIN to GND		-0.3 to 75 V
SW to GND		-0.3 to VIN
BS to GND		V_{SW}-0.3 to V_{SW}+6 V
HG, LG, VFB,EN to GND		-0.3 to 6 V
Max operating junction temperature(T_J)		125°C
Ambient temperature(T_A)		-40°C – 85°C
Package thermal resistance (θ_{JC})	SOP-8	45°C / W
Storage temperature(T_S)		-40°C – 150°C
Lead temperature & time		260°C, 10S
ESD (HBM)		>2000V

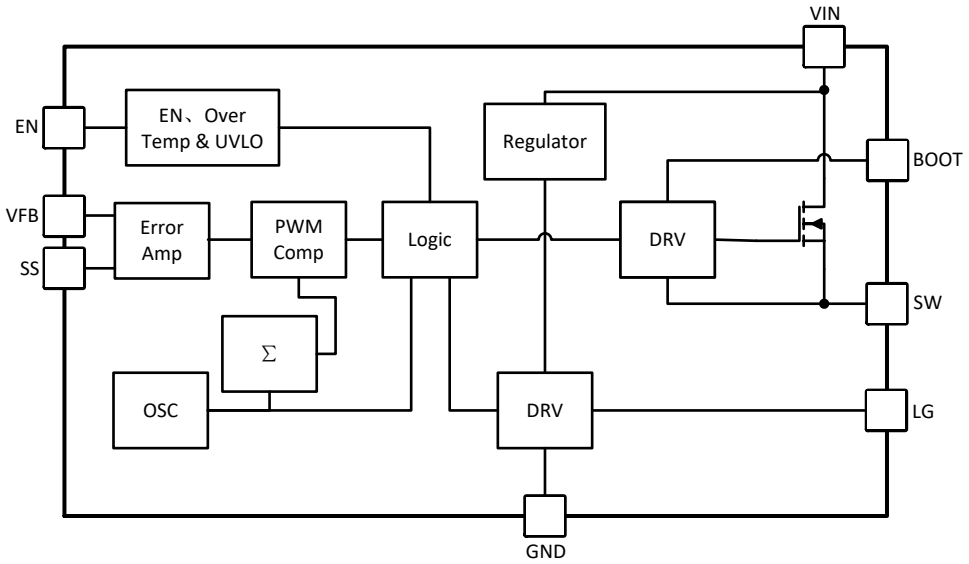
Note: *Exceed these limits to damage to the device. Exposure to absolute maximum rating conditions may affect device reliability.*

ELECTRICAL CHARACTERISTICS

(V_{IN}=12V, T_A=25℃, unless otherwise stated)

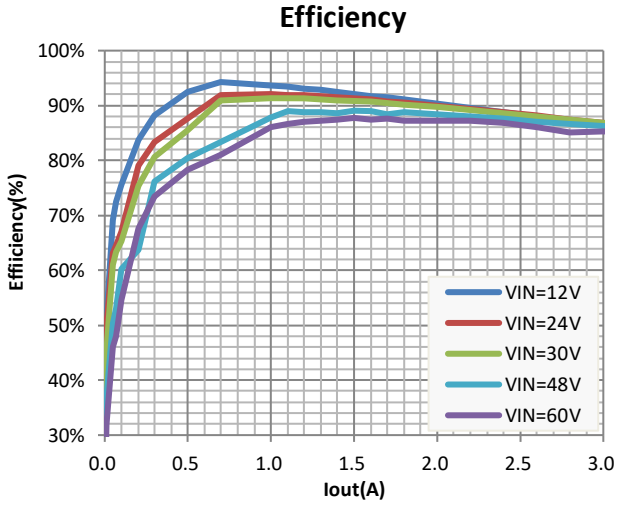
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage		7		70	V
V_{UVLO}	UVLO voltage			6.2		V
	UVLO hysteresis			0.8		V
I_{CCQ}	Quiescent current	V_{FB} = 1.1V, force driver off.		0.6	2.5	mA
I_{SB}	Standby current	No load, V_{IN}=12V,V_{OUT}=5V		0.6		mA
High side	RDS_{ON} Of Power MOS	I_{OUT}=1A		50		mΩ
V_{FB}	Feedback voltage		0.98	1	1.02	V
F_{SW}	Switching frequency	I_{OUT}=1A		150		KHz
D_{MAX}	Maximum duty cycle			91		%
	Minimum on-time			250		ns
V_{ENH}	EN high threshold			1.2		V
V_{ENL}	EN low threshold			0.7		V
I_{LIMIT}	Secondary cycle-by-cycle current limit	Minimum duty cycle, no CC		7		A
T_{SD}	Thermal shutdown temp			150		°C
T_{SH}	Thermal shutdown hysteresis			30		°C

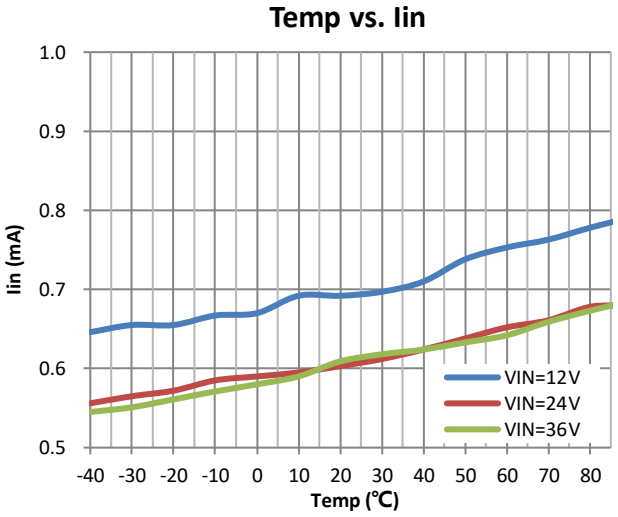
BLOCK DIAGRAM

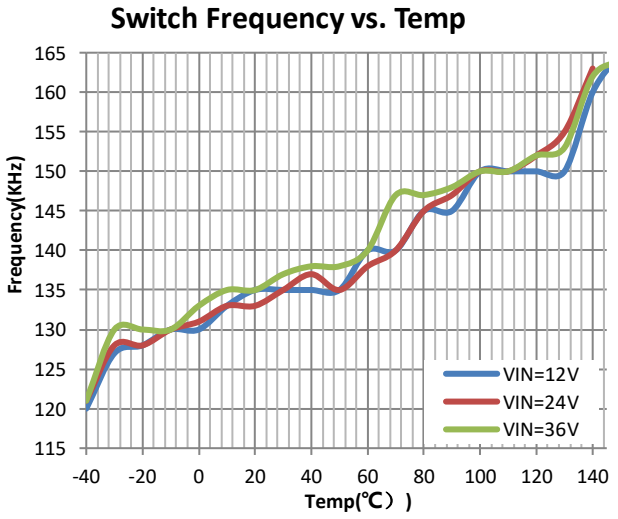


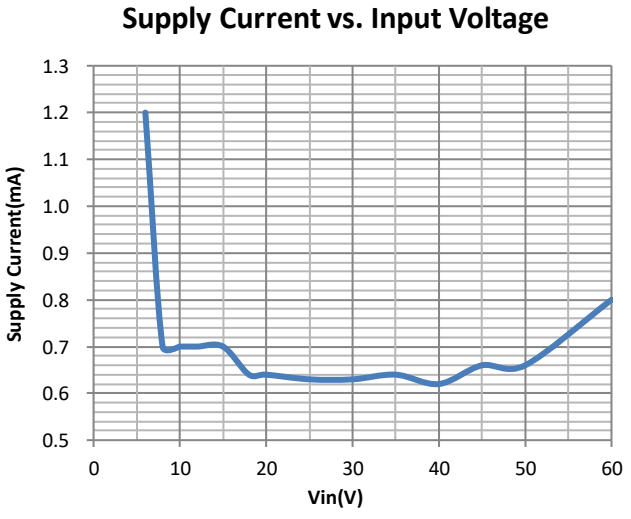
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{OUT}=5V)

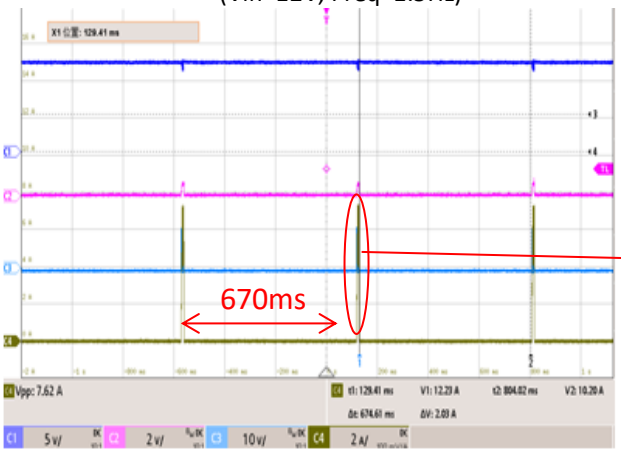






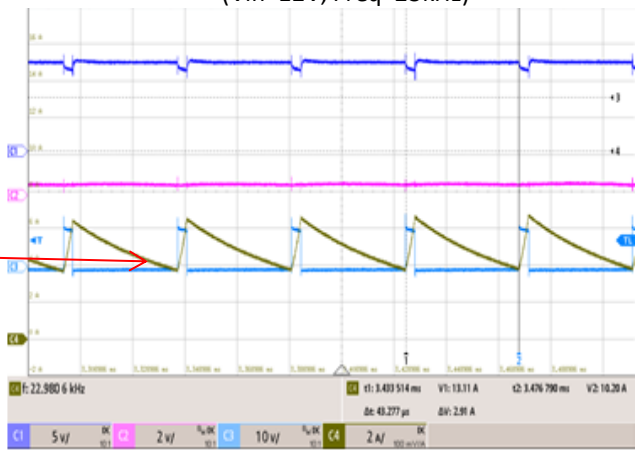


Short Circuit
(Vin=12V, Freq=1.5Hz)



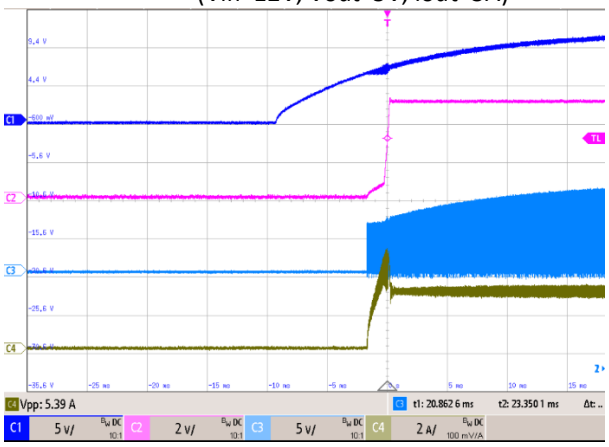
CH3: SW

Short Circuit
(Vin=12V, Freq=23kHz)



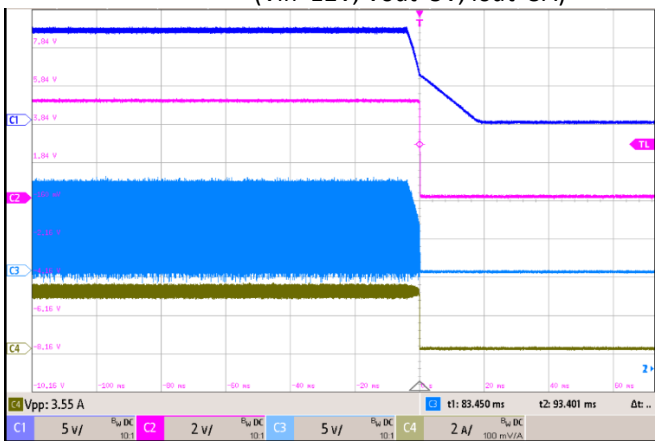
CH1: Vin, CH2: Vout, CH3: SW, CH4: Isw

Power On
(Vin=12V, Vout=5V, Iout=3A)



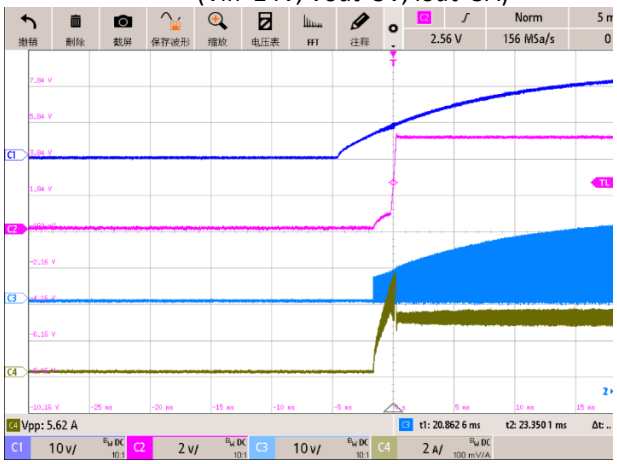
CH1: Vin, CH2: Vout, CH3: SW, CH4: Isw

Power Off
(Vin=12V, Vout=5V, Iout=3A)



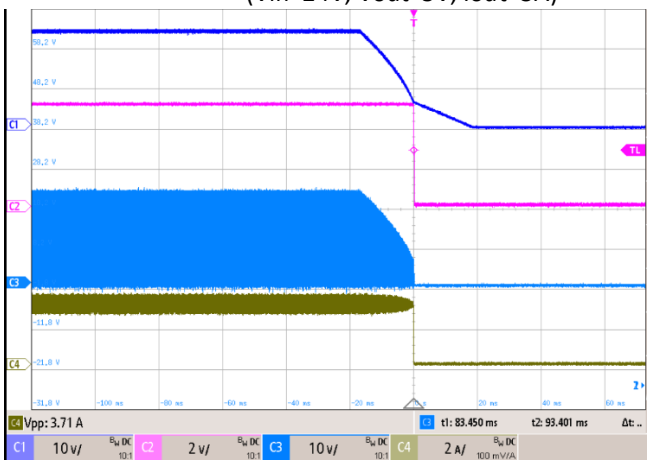
CH1: Vin, CH2: Vout, CH3: SW, CH4: Isw

Power On
(Vin=24V, Vout=5V, Iout=3A)



CH1: Vin, CH2: Vout, CH3: SW, CH4: Isw

Power Off
(Vin=24V, Vout=5V, Iout=3A)



CH1: Vin, CH2: Vout, CH3: SW, CH4: Isw

DETAILED DESCRIPTION

Input under voltage protection

BLL2683 provides an input voltage up to 70V and operates from an input voltage range of 7V to 70V. If VIN drops below 6.2V, the UVLO circuit inhibits switching. Once VIN rises above 7V, the UVLO clears, and the soft-start sequence activates.

Soft-start

BLL2683 has an External soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the soft-start circuitry slowly ramps up current available after 1ms. SS programming pin. Connect a capacitor from this pin to ground to program the soft start time.

$$T_{SS} = C_{SS} \times 1V/0.5uA$$

Constant voltage output

BLL2683 presets the V_{FB} voltage to 1V. The output voltage can be set by extra resistance.

Short circuit protection

When BLL2683 enter short circuit protection, the system will enter hit-cup mode, and frequency drop to 23KHZ per cycle and stop switching for 670mS.

Inductor selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{V_{OUT}}{f \times L}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor increased inductance requires more turns of wire and therefore copper losses will increase. Copper losses also increase as frequency increases Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates 'hard', which means that inductance collapses abruptly when the peak design current is exceeded. This result in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style Lower ripple current reduces power losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$\mathrm{L} = \frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

value, but is very dependent on the inductance selected. As the inductance or frequency increases, core losses decrease. Unfortunately, inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coil craft, Vishay, NEC/Tokin.

Input capacitor (CIN) selection

The input capacitance CIN is needed to filter the square wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN}=2V_{OUT}$, where:

$$I_{RMS} \cong I_{OUT(MAX)}/2$$

This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it

advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Output capacitor (COUT) selection

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, $\triangle V_{OUT}$, is determined by:

$$\Delta V_{OUT} < \Delta I_L \left(\frac{1}{8f \times C_{OUT}} + ESR \right)$$

The output ripple is highest at maximum input voltage since $\triangle I_L$ increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints.

Thermal shutdown

The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 150°C), the converter shuts off. This is non-latch protection. There is about 30°C hysteresis. Once the junction temperature drops around 120°C, it initiates a Soft-start.

TYPICAL APPLICATION CIRCUITS

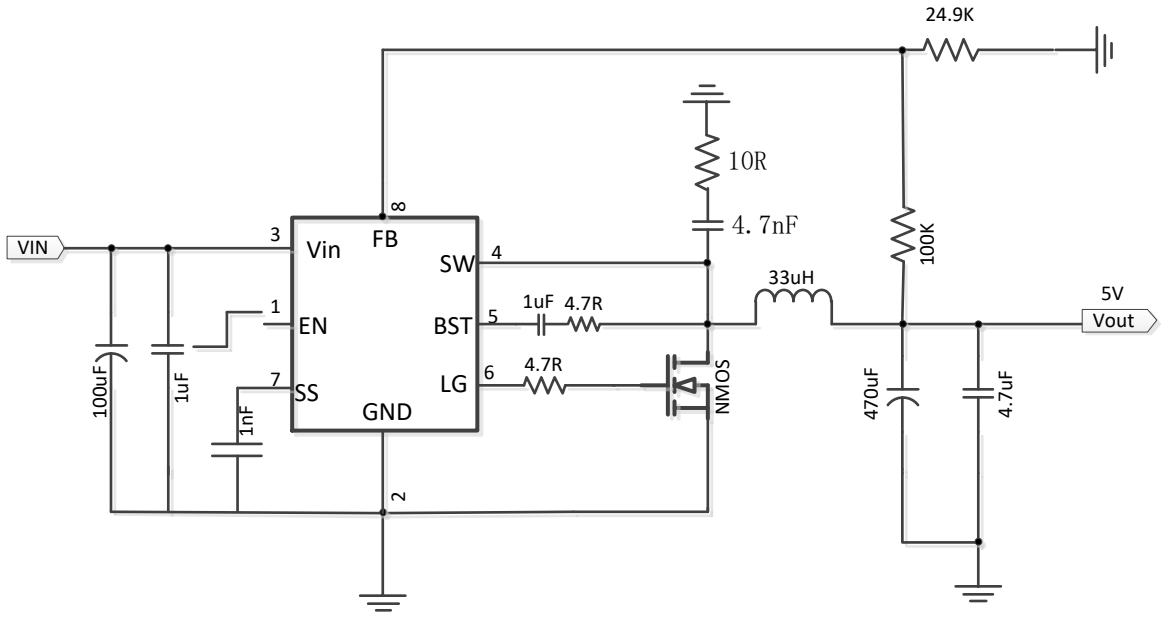


Figure3. 12V-70V VIN, 5V/3A

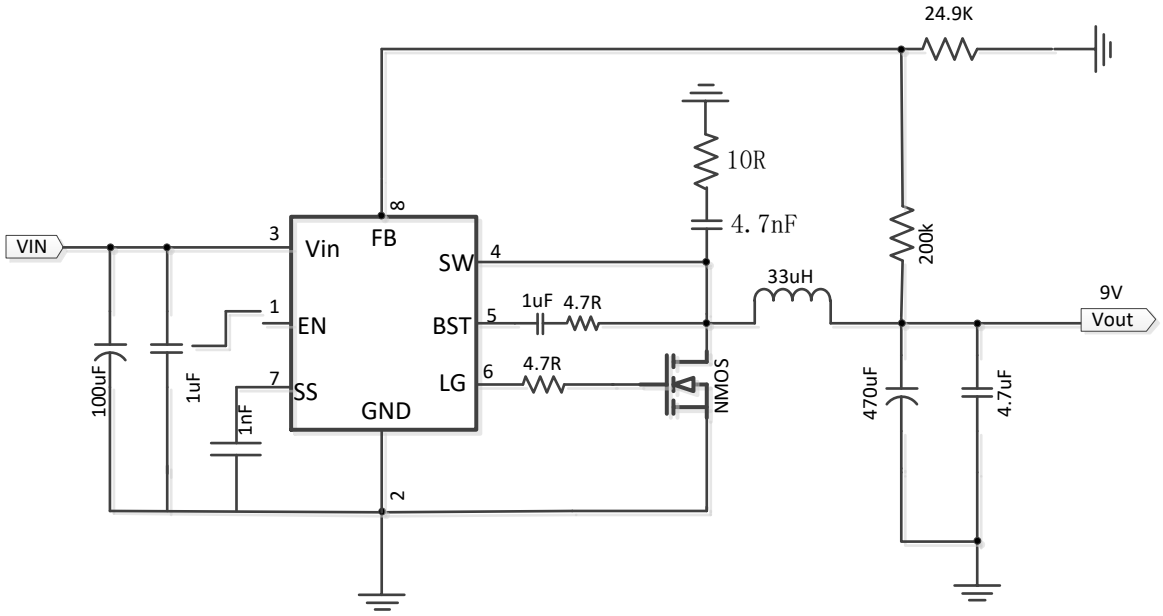


Figure4. 12V-70V VIN, 9V/3A

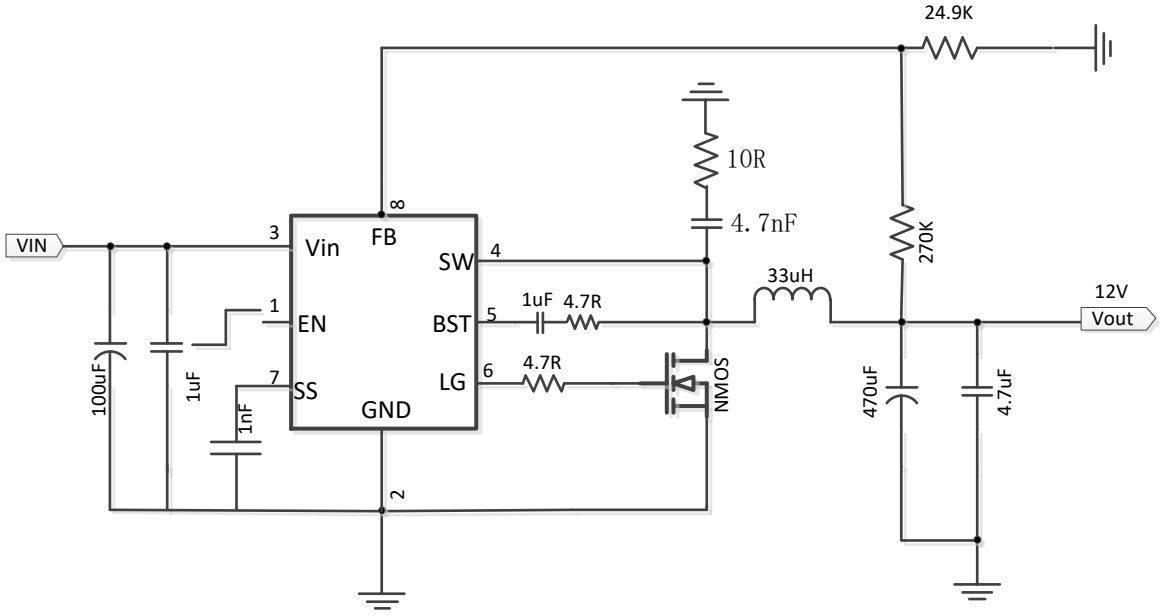
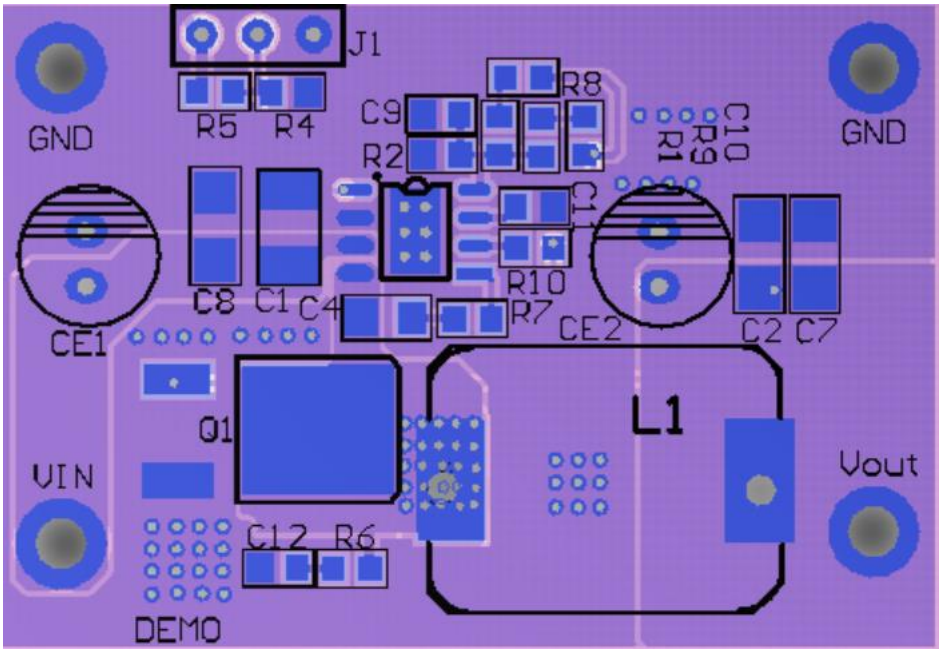


Figure5. 14V-70V VIN, 12V/3A

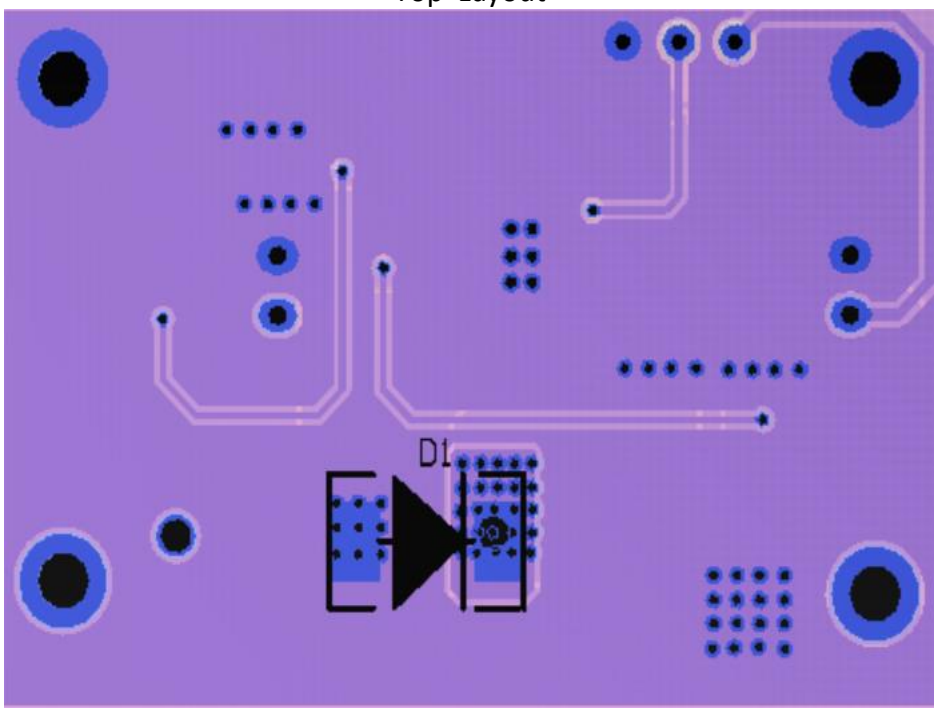
LAYOUT GUIDE

PCB layout is very important to achieve stable operation. For best results, use the following guidelines and figures as reference.

1) Keep the connection between the input ground and GND pin as short and wide as possible.
2) Keep the connection between the input capacitor and VIN pin as short and wide as possible.
3) Use short and direct feedback connections. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.



Top Layout

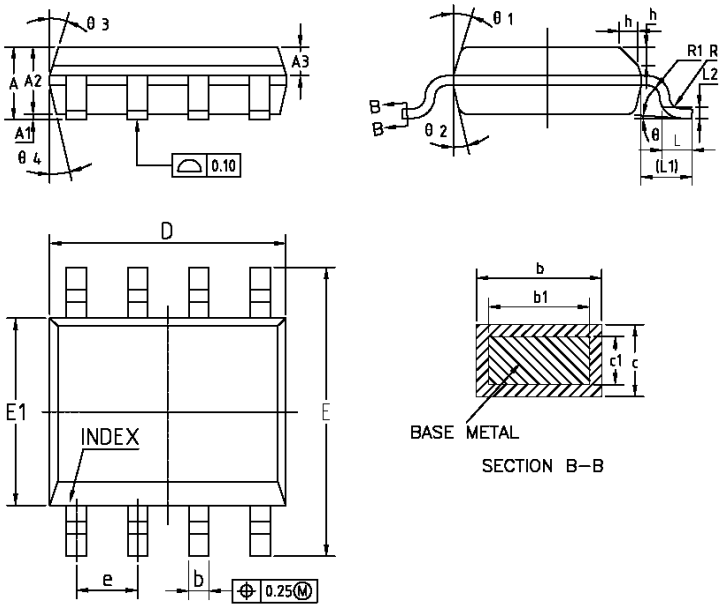


Bottom Layout

PACKAGE OUTLINE

Package	SOP-8	Devices per reel	4000pcs

Package specification：



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	–	0.51
b1	0.37	0.42	0.47
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ 1	15°	17°	19°
θ 2	11°	13°	15°
θ 3	15°	17°	19°
θ 4	11°	13°	15°

Unit: mm